AMENDMENT TO THE CLAIMS

Please **ADD** claims 23-31 as follows.

A copy of all pending claims and a status of the claims is provided below.

Claims 1 – 8. (Canceled).

9. (Previously presented) A semiconductor structure formed on a substrate, comprising:

an n-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain;

a first shallow trench isolation for the n-channel field effect transistor comprising a first shallow trench isolation side, the first shallow trench isolation side having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the n-channel field effect transistor,

the first shallow trench isolation for the n-channel field effect transistor further comprising a second shallow trench isolation side being transverse to the first shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-channel field effect transistor;

a p-channel field effect transistor, the p-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain;

a second shallow trench isolation for the p-channel field effect transistor having a third shallow trench isolation side, the third shallow trench isolation side being devoid of

an overhang; and

the second shallow trench isolation for the p-channel field effect transistor further having a fourth shallow trench isolation side, the fourth shallow trench isolation side being transverse to the third shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the p-channel field effect transistor.

10. (Original) The semiconductor structure of claim 9, wherein the overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow prevents a degradation of hole mobility.

11. (Original) The semiconductor structure of claim 9, wherein:

the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the first shallow trench isolation would affect performance of the n-channel field effect transistor, and

the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the second shallow trench isolation would affect performance of the n-channel field effect transistor.

Claims 12 - 14. (Canceled).

15. (Original) The semiconductor structure of claim 9, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side for the second shallow trench isolation for the p-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the fourth shallow trench isolation side would affect performance of the p-channel field effect transistor.

16. (Original) The semiconductor structure of claim 15, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side is less than or equal to about 5.0 microns.

17. (Original) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side is less than or equal to about 5.0 microns.

18. (Previously Presented) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side is less than or equal to about 5.0 microns.

Claims 19 – 22. (Canceled).

23. (New) A semiconductor structure, comprising:

an first transistor having a first shallow trench isolation having:

a side with at least one overhang configured to prevent oxidation induced stress in a direction parallel to a direction of current flow; and

a transverse side having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the first transistor;

a second transistor with a shallow trench isolation having:

a side devoid of an overhang; and

a traverse side having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the second transistor, wherein

the at least one overhang of the first transistor and the second transistor are provided when a distance between an STI and one of the first transistor and the second transistor is less than or equal to a predetermined distance which varies based on at least one of thermal mismatch between isolation, dielectric and silicon substrate and intrinsic stress of a nitride mask used to form the semiconductor structure.

24. (New) The semiconductor structure of claim 23, wherein the first transistor is an n-channel field effect transistor and the second transistor is a p-channel field effect transistor.

25. (New) The semiconductor structure of claim 24, wherein the n-channel field effect transistor and the p-channel field effect transistor have a source, a drain, a gate, and the direction of current flow is from the source to the drain.

26. (New) The semiconductor structure of claim 23, wherein the overhang of the

first and second transistor configured to prevent oxidation induced stress in a direction transverse to the direction of current flow prevents a degradation of hole mobility.

27. (New) The semiconductor structure of claim 23, wherein the predetermined distance is a distance from a gate of the first transistor to the side of the shallow trench isolation for the first transistor which is less than or equal to a distance within which oxidation induced stress adjacent to the shallow trench isolation would affect performance of the n-channel field effect transistor.

28. (New) The semiconductor structure of claim 23, wherein the predetermined distance is a distance from a gate of the first transistor to the transverse side of the shallow trench isolation for the first transistor which is less than or equal to a distance within which oxidation induced stress adjacent to the shallow trench isolation would affect performance of the n-channel field effect transistor.

29. (New) The semiconductor structure of claim 23, wherein the predetermined distance is a distance from a gate of the second transistor to the transverse side for the shallow trench isolation for the second transistor which is less than or equal to a distance within which oxidation induced stress adjacent to the transverse side would affect performance of the p-channel field effect transistor.

30 (New) The semiconductor structure of claim 29, wherein the distance from the gate of the second transistor to the transverse side is less than or equal to about 5.0

microns.

31. (New) The semiconductor structure of claim 28, wherein the distance from the gate of the first transistor to the side of the shallow trench isolation of the first transistor is less than or equal to about 5.0 microns.